PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

Jae-jun MOON, et al.

Appln. No.: 10/777,097

Confirmation No.: 4555

Filed: February 13, 2004

For: BIAS CIRCUIT HAVING START-UP CIRCUIT

Docket No: Q77183

Group Art Unit: 2816

Examiner: Jeffery Shawn Zweizig

SUBMISSION OF APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find an Appeal Brief. A check for the statutory fee of $500.00 is attached. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this paper is attached.

Respectfully submitted,

/ Seok-Won Stuart Lee /

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Date: January 18, 2007

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, , Appellant hereby submits this Appeal Brief, appealing the final Office Action dated August 18, 2006 (hereinafter "the final Office Action), finally rejecting claims 1-10. This Appeal Brief is accompanied by a Submission including the required appeal fee set forth in 37 C.F.R. § 41.20(b)(2) and a Petition for a 1-Month Extension of Time. Appellant's Notice of Appeal was filed on October 18, 2006. Therefore, the present Appeal Brief is timely filed.

01/19/2007 MAHMED1 00000071 10777097
01 FC:1251 120.00 OP

01/19/2007 MAHMED1 00000071 10777097
02 FC:1402 500.00 OP

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I. REAL PARTY IN INTEREST

The real party in interest is SAMSUNG ELECTRONICS CO., LTD., (Assignee) by virtue of an assignment executed by the inventors (Appellant), Jae-jun MOON, Jeong-won LEE, and Jung-eun LEE, on February 5, 2004, and recorded by the Assignment Branch of the U.S. Patent and Trademark Office on February 13, 2004 (at Reel 014989, Frame 0832).

II. RELATED APPEALS AND INTERFERENCES

Applicant submits that the present application was previously subject to appeal. The claims were twice rejected in a prior Final Office issued August 30, 2005. In response, the Applicant filed a Notice of Appeal on November 30, 2005, and an Appeal Brief on February 28, 2006.

After the filing of the February 28, 2006 Appeal Brief, the prosecution of the present application was reopened when the PTO issued a Non-Final Office Action on March 17, 2006. After filing an Amendment on July 17, 2006, a Final Office Action was issued on August 18, 2006, and the present Appeal is based on the August 18, 2006 Final Office Action.

Upon information and belief, there are no other pending appeals, interferences, or judicial proceedings known to Appellant, Appellant's representatives or the Assignee that may be related to, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-10 are all the claims pending in the application.

Claim 4 is objected to for reciting "a second common node" on line 13, when the claim should recite --the second common node--.[1]

Claims 1,3 and 5-9 are rejected under 35 U.S.C. § 102(b) as being anticipated by Wu et. al (U.S. Patent No. 5,307,007; hereinafter "Wu").

Claims 1-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki (U.S. Patent No. 5,180,967; hereinafter "Yamazaki") in view of Wu.

Claims 1-10, which have been at least twice rejected, are the claims on appeal (See Claims Appendix).

[1] Applicant submits that the Office Action is correct in that claim 4 should recite --the second common node-- on line 13, and agrees to amend claim 4 or request an Examiner's amendment to replace "a second common node" with --the second common node-- upon the conclusion of this Appeal. Applicant respectfully submits that the aforementioned informality in claim 4 has no bearing on Applicant's appeal of the Examiner's rejection of claims 1-10 over prior art.

IV. STATUS OF AMENDMENTS

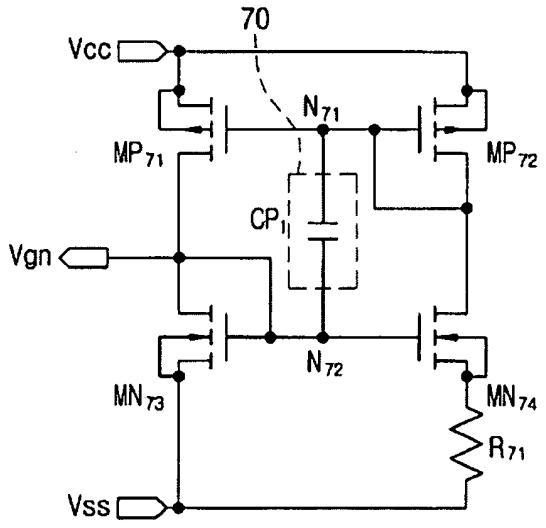
The claims on appeal, claims 1-10, have not been amended subsequent to the final rejection of August 18, 2006.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention relates to a bias circuit having a start-up circuit. See Abstract of Appellant's Specification. The start-up circuit prevents noise caused by power source voltage and power consumption due to static currents and provides improved stability at high frequencies. See id.

An embodiment of the bias circuit shown in Fig. 7 is reproduced below:

FIG. 7



Claims 1 and 2

An embodiment of the present invention provides a bias circuit having a bias circuit part and a start-up circuit. The bias circuit part uses a current mirror circuit and generates a constant bias voltage at an output node from a power source as applied.

The embodiment further includes a start-up circuit having a capacitor connected between the output node and a common node of in common connecting gates of MOS transistors constructing the current mirror circuit.

Claims 3 and 4

Another embodiment of the invention includes a bias circuit having a bias circuit part and a start-up circuit part. The bias circuit part uses a cascode current mirror circuit of a double-stage current mirror circuit and generates a constant bias voltage to an output node from an applied power source voltage.

The start-up circuit part actuates the bias circuit part upon an initial application of the power source voltage. The start-up circuit part includes a first capacitor and a second capacitor.

The first capacitor is connected between a first common node and a second common node. The first common node connects in common gates of first MOS transistors constructing a first single-stage current mirror circuit of the cascode current mirror circuit. The second common node connects in common gates of second MOS transistors constructing a second single-stage current mirror circuit.

There is also a second capacitor connected between the second common node and the output node.

Means-Plus-Function Claims

No means-plus-function or step-plus-function has been identified among the claims on appeal.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 3 and 5-9 are rejected under 35 U.S.C. § 102(b) as being anticipated by Wu et al. (U.S. Patent No. 5,307,007; hereinafter "Wu").

2. Claims 1-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki (U.S. Patent No. 5,180,967; hereinafter "Yamazaki") in view of Wu.

VII. ARGUMENT

1. Rejection of Claims 1, 3 and 5-9 Under § 102(b) By Wu

Applicant respectfully submits that claim 1 is patentable because Wu fails to disclose each and every element of the claim. Claim 1 recites:

> A bias circuit having a start-up circuit, comprising:
>
> a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output node from a power source voltage as applied, and
>
> a start-up circuit part having a capacitor connected between the output node and a common node of in common connecting gates of MOS transistors constructing the current mirror circuit.

(Emphasis added).

Applicant submits that Wu fails to disclose or suggest, inter alia, a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output node from a power source voltage as applied, and a start-up circuit part having a capacitor connected between the output node and a common node the bias circuit and the start-up circuit, as recited in the claim.

In the Final Office Action, the Examiner states that the node between the NMOS transistors M1 and M3 corresponds to the claimed output node. See paragraph 2 at page 2. First, this particular node at the gate of NMOS transistor M3 cannot correspond to the claimed output node. This particular node is merely connected to the gate of PMOS transistor M1, the gate of the NMOS transistor M3, the gate of the NMOS transistor M4, the capacitor C_1, the

source/drains of the NMOS transistor M3 and M4, and the gates of transistors M5 and M6. Therefore, there the gate of MOS transistor M3 does not provide any sort of output, and thus, cannot possibly correspond to the claimed output node.

Applicant points out that in a description of an embodiment of the invention, "an output voltage Vgn is outputted through the output node." Paragraph 43 of Specification and Fig. 7. In contrast, there is absolutely nothing at the gate of the NMOS transistor M3 which would allow the output or the detection of any voltage at the gate.

Second, the Examiner's argument that the gate of M3 corresponds to the claimed output node ignores the recitations of claim 1. In claim 1, the start-up circuit part is recited as having a common node of in common connecting gates of MOS transistors and separately recites an output node to which a constant bias voltage is generated. In other words, the gate of M3 may correspond to a type of a common node, but does not correspond to an output node. Therefore, the characterization of the gate of M3 as corresponding to the claimed output node ignores the fine distinctions made by the Applicants in the claim language.

Not only does Wu fail to expressly disclose an output node, Wu also fails to inherently disclose an output node.

"To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." M.P.E.P. § 2112(IV) (quoting In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Moreover, "[t]he fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish

the inherency of that result or characteristic." Id. (quoting In re Rijckaert, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art)).

In the Office Action, a basis or a technical reasoning for having the claimed output node in Wu is not provided. For example, there is no rationale for outputting a voltage at the node between the NMOS transistors M1 and M3 to reasonably support the determination that the output node of claim 1 is necessarily present in Wu.

Admittedly, Wu does disclose outputting a voltage level, i.e., V_{out}, but this particular voltage is outputted at an entirely different location at the transistor Q_3 as shown in Fig. 1. Here, the mere fact that there may be an output node at the gate of NMOS transistor M3, when such a node is clearly not disclosed, is not sufficient to support an inherent disclosure of the claimed output node in Wu. Since Wu fails to disclose or suggest all claim elements, claim 1 is not anticipated by Wu and thus, patentable.

For reasons similar to those submitted for claim 1, claims 3 and 9 are patentable. For example, Wu fails to disclose or suggest a bias circuit comprising, inter alia, a bias circuit part using a cascode current mirror circuit of a double-stage current mirror circuit, and for generating a constant bias voltage to an output node from an applied power source voltage (claim 3) or a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output terminal node from a power source voltage as applied (claim 9).

Claims 5 and 7, which depend from claim 1, and claims 6 and 8, which depend from claim 3, are patentable for at least the reasons submitted for their respective base claims.

2. Rejections of Claims 1-10 under § 103(a) over Yamazaki in view of Wu

Applicant respectfully submits that claim 1 is patentable because Yamazaki in view of Wu fails to teach, suggest or provide motivation for, inter alia, the claimed output node as recited in the claim. Although the Examiner cites nodes N11 or N12 of Yamazaki as allegedly corresponding to the claimed output node, there is nothing in Yamazaki that suggests that these nodes are output nodes. Instead, the node N11 is merely connected to the drain and the gate of the PMOS 104, the gate of the PMOS 106, the gate of the PMOS transistor 116, the drain of the NMOS transistor 118, and the drain of the NMOS transistor 112. Node N12 is merely connected to the drain of the PMOS transistor 105, the drain of the PMOS transistor 120, and the gate and the drain of the NMOS transistor 110.

In addition, there is nothing in the references or in the Final Office Action which supports the conclusion that the claimed output node is necessarily present in the combination of Yamazaki and Wu. Therefore, Yamazaki in view of Wu cannot inherently disclose such an output node.

Applicant also submits that a prima facie case of obviousness has not been established. On pages 4-5 of the Final Office Action, the Examiner proffers that it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the sixth transistor 118 and the seventh transistor 120 of Yamazaki with the capacitor C1 of Wu. The motivation for such a combination, according to the Examiner, would be for reducing component count and static current consumption. Applicant disagrees and submits that such a reasoning relies on improper hindsight. One cannot use hindsight reconstruction to pick and choose among

disclosures in the prior art to deprecate the claimed invention. See In re Fine, U.S.P.Q. 2d 1596 (Fed. Cir. 1988).

Moreover, there is nothing in Yamazaki which teaches or suggests generating a constant bias voltage, as claimed, as there is nothing in Yamazaki which even suggests an improvement in the stability of a bias voltage.

For at least the above reasons, claim 1 is patentable.

For reasons similar to those submitted for claim 1, independent claims 3 and 9 are patentable. Specifically, claims 3 and 9 are patentable because Yamazaki fails to teach or suggest an output node (claim 3) and an output terminal node (claim 9), respectively, as recited in the claim.

Claims 2, 5 and 7, which depend from claim 1, claims 4, 6 and 8, which depend from claim 3, and claim 10, which depends from claim 9, are patentable for at least the reasons submitted for their respective base claims.

In addition, claim 4 is further patentable because Yamazaki fails to teach or suggest the first NMOS transistor and the second NMOS transistor as claimed. Claim 4 recites:

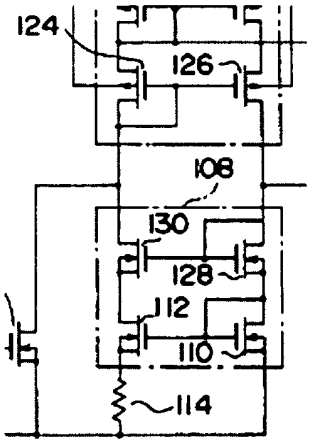
> a first NMOS transistor having a drain and a gate thereof connected to a drain of the third PMOS transistor to form the output node, . . . ;
>
> a second NMOS transistor having a drain thereof connected to the drain of the fourth PMOS transistor . . . .

In the Final Office Action, the Examiner alleges that the following transistors of Yamazaki correspond to the following claim elements:

Claim Element	Cited Transistors in Fig. 5 of Yamazaki (See page 5 of Final Office Action)
first NMOS transistor	third NMOS transistor 110
third PMOS transistor	eighth PMOS transistor 126

However, the piece-by-piece matching of individual claim elements with disparate teachings of Yamazaki ignores the recitations of the claim elements.

As noted above, claim 4 recites a first NMOS transistor having a drain and a gate thereof connected to a drain of the third PMOS transistor to form the output node, in combination with other elements of the claim. In Yamazaki, the drain and the gate of third NMOS transistor 110 are not connected to the drain of the eighth PMOS transistor 126. Rather, the drain and the gate of the third NMOS transistor 110 are connected to the source of the tenth NMOS transistor 128. For clarity, the relevant portion of Fig 5 is reproduced on the right.



Portion of Fig. 5 of Yamazaki

Further, the Examiner argues that the following claim elements correspond to the cited transistors of Yamazaki:

Claim Element	Cited Transistors in Fig. 5 of Yamazaki (See page 5 of Final Office Action)
second NMOS transistor	fourth NMOS transistor 112
fourth PMOS transistor	ninth PMOS transistor 124

Here, the drain of the fourth NMOS transistor 112 is not connected to the drain of the ninth PMOS transistor 124, as shown in Fig. 5. Rather, the drain of the fourth NMOS transistor 112 is connected to the source of the eleventh NMOS transistor 130.

Therefore, claim 4 is additionally patentable because Yamazaki fails to teach or suggest the claimed first and the second NMOS transistors.

For reasons similar to those submitted for claim 4, claim 10 is additionally patentable.

VIII. CONCLUSION

In view of the foregoing, Appellant submits that the Examiner has failed to show how claims 1, 3 and 5-9 are anticipated and to establish a prima facie case of obviousness with respect to claims 1-10. Therefore, the rejection of claims 1-10 under 35 U.S.C. § 102(b) and 103(a) is improper and should be reversed.

Unless a check is submitted herewith for the fee required under 37 C.F.R. §41.37(a) and 1.17(c), please charge said fee to Deposit Account No. 19-4880.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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Date: January 18, 2007

CLAIMS APPENDIX

CLAIMS 1-10 ON APPEAL:

1. A bias circuit having a start-up circuit, comprising:

a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output node from a power source voltage as applied, and

a start-up circuit part having a capacitor connected between the output node and a common node of in common connecting gates of MOS transistors constructing the current mirror circuit.

2. The bias circuit as claimed in claim 1, wherein the MOS transistors include a first PMOS transistor and a second PMOS transistor and the bias circuit part includes:

the first PMOS transistor having a source thereof connected to the power source voltage;

the second PMOS transistor having a gate and a drain thereof connected to a gate of the first PMOS transistor to form the common node, and having a source thereof connected to the power source voltage;

a first NMOS transistor having a drain and a gate thereof connected to a drain of the first PMOS transistor to form the output node, and having a source thereof connected to a grounded power source;

a second NMOS transistor having a drain thereof connected to the drain of the second PMOS transistor, and having a gate thereof connected to the gate of the first NMOS transistor; and

a resistor connected between the source of the second NMOS transistor and the grounded power source.

3. A bias circuit having a start-up circuit, comprising:

a bias circuit part using a cascode current mirror circuit of a double-stage current mirror circuit, and for generating a constant bias voltage to an output node from an applied power source voltage; and

a start-up circuit part for actuating the bias circuit part upon an initial application of the power source voltage, the start-up circuit part including:

a first capacitor connected between a first common node connecting in common gates of first MOS transistors constructing a first single-stage current mirror circuit of the cascode current mirror circuit and a second common node connecting in common gates of second MOS transistors constructing a second single-stage current mirror circuit; and

a second capacitor connected between the second common node and the output node.

4. The bias circuit as claimed in claim 3, wherein the first MOS transistors include a first PMOS transistor and a second PMOS transistor, the second MOS transistors include a third PMOS transistor and a fourth PMOS transistor and the bias circuit part includes:

the first PMOS transistor having a source thereof connected to the power source voltage;

the second PMOS transistor having a gate and a drain thereof connected to a gate of the first PMOS transistor to form the first common node, and having a source thereof connected to the power source voltage;

the third PMOS transistor having a source thereof connected to a drain of the first PMOS transistor;

the fourth PMOS transistor having a gate and a drain thereof connected to a gate of the third PMOS transistor to form a second common node, and having a source thereof connected to the drain of the second PMOS transistor;

a first NMOS transistor having a drain and a gate thereof connected to a drain of the third PMOS transistor to form the output node, and having a source thereof connected to a grounded power source;

a second NMOS transistor having a drain thereof connected to the drain of the fourth PMOS transistor, and having a gate thereof connected to the gate of the first NMOS transistor; and

a resistor connected between a source of the second NMOS transistor and the grounded power source.

5. The bias circuit as claimed in claim 1, wherein the output node outputs the constant bias voltage out of the bias circuit.

6. The bias circuit as claimed in claim 3, wherein the output node outputs the constant bias voltage out of the bias circuit.

7. The bias circuit as claimed in claim 1, wherein the output node outputs the constant bias voltage to another circuit outside the bias circuit.

8. The bias circuit as claimed in claim 3, wherein the output node outputs the constant bias voltage to another circuit outside the bias circuit.

9. A bias circuit having a start-up circuit, comprising:

a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output terminal node from a power source voltage as applied, and

a start-up circuit part having a capacitor connected between a base of the output terminal and a common node of in common connecting gates of MOS transistors constructing the current mirror circuit.

10. The bias circuit as claimed in claim 9, wherein the MOS transistors include a first PMOS transistor and a second PMOS transistor and the bias circuit part includes:

the first PMOS transistor having a source thereof connected to the power source voltage;

the second PMOS transistor having a gate and a drain thereof connected to a gate of the first PMOS transistor to form the common node, and having a source thereof connected to the power source voltage;

a first NMOS transistor having a drain and a gate thereof connected to a drain of the first PMOS transistor to form the base of the output terminal, and having a source thereof connected to a grounded power source;

a second NMOS transistor having a drain thereof connected to the drain of the second PMOS transistor, and having a gate thereof connected to the gate of the first NMOS transistor; and

a resistor connected between the source of the second NMOS transistor and the grounded power source.

EVIDENCE APPENDIX:

This Appendix is not applicable to this Appeal.

RELATED PROCEEDINGS APPENDIX

This Appendix is not applicable to this Appeal.